What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate; and

a dielectric layer formed over the semiconductor substrate and having a first portion formed with an amorphous material and a second portion formed with a monocrystalline material, where an electric field in the dielectric layer controls a conductivity of the semiconductor substrate.

2. The semiconductor device of claim 1, further comprising a control electrode overlying the dielectric layer for establishing the electric field between the control electrode and the semiconductor substrate.

3. The semiconductor device of claim 2, further comprising:

a drain; and

a source, where the electric field generates a conduction channel in the substrate to couple the drain to the source.

4. The semiconductor device of claim 1, wherein the first portion of the dielectric layer is formed adjacent to the semiconductor substrate and the second portion of the dielectric layer is formed between the first portion and the control electrode.

5. The semiconductor device of claim 1, wherein the amorphous material includes silicon dioxide.

6. The semiconductor device of claim 1, wherein the monocrystalline material includes a material selected from the group consisting of barium, strontium, titanium, lanthanum, zirconium, aluminum and oxygen.

7. The semiconductor device of claim 1, wherein the first portion of the dielectric layer has a relative permittivity less than ten and the second portion of the dielectric layer has a relative permittivity greater than thirty.

8. The semiconductor device of claim 7, wherein the dielectric layer is formed with a thickness greater than thirty angstroms.

9. A transistor, comprising:

a substrate;

a gate electrode disposed over the substrate for generating a conduction channel in the substrate in response to a control signal; and

a dielectric formed over the conduction channel, the dielectric including a first layer formed with an amorphous material, a second layer formed with a monocrystalline material disposed between the first layer and the gate electrode.

10. The transistor of claim 9, further comprising a source and a drain, where the conduction channel couples the source to the drain to control a current of the transistor.

11. The transistor of claim 10, wherein a length of the conduction channel is less than one hundred nanometers.

12. The transistor of claim 9, wherein the monocrystalline material has a higher permittivity than the amorphous material.

13. The transistor of claim 9, wherein the dielectric is formed with a thickness greater than thirty angstroms.

14. A method of operating a transistor, comprising the steps of:

providing a gate dielectric overlying a semiconductor substrate; and

applying a control signal to generate a first field in an amorphous layer of the gate dielectric and a second field in a monocrystalline layer of the gate dielectric.

15. The method of claim 14, further comprising the step of generating a conduction path of the transistor in the semiconductor substrate with the control signal.

16. The method of claim 14, wherein the step of applying includes the step of generating the first field adjacent to the semiconductor substrate.

17. The method of claim 14, wherein the step of applying includes the step of polarizing the gate dielectric with the control signal.

18. The method of claim 17, wherein the step of polarizing includes the step of polarizing silicon dioxide with the first field.

19. The method of claim 17, wherein the step of polarizing includes the step of polarizing a material based on the group consisting of barium, strontium, titanium, lanthanum, zirconium, aluminum and oxygen with the second field.

20. The method of claim 14, further comprising the steps of:

polarizing the amorphous layer to generate a first polarization field; and

polarizing the monocrystalline layer to generate a second polarization field greater than the first polarization field.